BAKER BOTTS LLP

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35.U.S.C. 371

EXPRESS MAIL LABEL No.	DATE
EF321684927US	21 JUNE 2001

ATTORNEY'S DOCKET NO. A34394 PCT USA

U.S. APPLICATION NO. 09/868797

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE99/04050	21 DECEMBER 1999	22 DECEMBER 1998

TITLE OF INVENTION: DEVICE AND METHOD FOR GENERATING AND EXECUTING COMPRESSED PROGRAM OF A VERY LONG INSTRUCTION WORD PROCESSOR

APPLICANT(S) FOR DO/EO/US: Matthias Weiss

Applicant herewith submits to the United States Designated /Elected Office (DO/EO/US) the following items and other information:

1. ☑ This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371.
3. ☑ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(I).
4. [ ] A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. [ ] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [ ] is transmitted herewith (required only if not transmitted by the International Bureau).
   b. [ ] has been transmitted by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☑ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. [ ] A copy of the International Search Report (PCT/ISA/210)
   a. [ ] are transmitted herewith (required only if not transmitted by the International Bureau).
   b. [ ] have been transmitted by the International Bureau
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.
8. [ ] A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. [ ] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☑ A copy of the International Preliminary Examination Report (PCT/IPEA/409)
12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☑ A FIRST preliminary amendment.
    [ ] A SECOND or SUBSEQUENT preliminary amendment.
14. [ ] A substitute specification.
15. [ ] A change of power of attorney and/or address letter.
16. ☑ Other items or information:
    a. ☑ a copy of the International Search Report (PCT/ISA/210)
    b. ☑ a copy of the International Preliminary Examination Report (PCT/IPEA/409)

Translation of Supplement Examination Report
Copy of International Application as published WO 00/38049
EnGlish translation (incl. 2 sheets drawings, 10 sheets of spec)
PCT/IPEA/416
PCT/ISA/220

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE99/04056 09/868797	21 DECEMBER 1999	22 DECEMBER 1998

17. ☑ The following fees are submitted:

Basic National Fee (37 CFR 1.492(a)(1)-(5):

Neither international preliminary examination fee (37 CFR 1.482)

Nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO (1.492(a)(3)) $1,000.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO (1.492(a)(5) $860.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO(1.492(a)(2)) $710.00

International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) (1.492(a)(1)) $690.00

International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) $ 100.00

CALCULATIONS PTO USE ONLY

ENTER APPROPRIATE BASIC FEE AMOUNT =				$ 860	
Surcharge of $130.00 for furnishing the oath or declaration later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 C.F.R. 1.492(e)).				$	
Claims	**Number Filed**	**Number Extra**	**Rate**	$	
Total Claims	10 -20=	0	X $ 18.00	$ 0	
Independent Claims	1 -3=	0	X $ 80.00	$ 0	
Multiple dependent claim(s) (if applicable)			+ $270.00	$	
TOTAL OF ABOVE CALCULATIONS =				$ 860	
Reduction by ½ for filing by small entity, if applicable.				$	
SUBTOTAL =				$ 860	
Processing fee of $130.00 for furnishing the English translation later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
TOTAL NATIONAL FEE =				$ 860	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property +				$	
TOTAL FEES ENCLOSED =				$ 860	
				Amt. refunded	$
				charged	$

a. ☑ A check in the amount of $ 860 to cover the above fees is enclosed.

b. [ ] Please charge our Deposit Account No. 02-4377 in amount of $_____ to cover the above fees. A copy of this sheet is enclosed.

c. ☑ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 02-4377. A copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:
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21 JUNE 2001
Date

BAKER BOTTS LLP

Attorney Docket Number: A34394 PCT USA

Title: DEVICE AND METHOD FOR GENERATING AND EXECUTING COMPRESSED PROGRAM OF A VERY LONG INSTRUCTION WORD PROCESSOR

Use Space Below for Additional Information:

PTO is the application which the inventor executed by signing the oath or declaration.

Also enclosed are:

1.	(x)	A check in the amount of	$ 130
	(x)	$130 - Other than Small Entity	
	( )	$ 65 - Small Entity	
		representing payment of the surcharge due for late filing of the Declaration pursuant to 37 C.F.R. 1.492(e);	
2.	()	An extension of time to file the Response to Missing Parts is respectfully requested. The required fee, calculated pursuant to 1.136(a), is enclosed in the amount of	$
3.	( )	Other _____	$
		TOTAL FEE ENCLOSED	$ 130

Enclosed: Form PCT/DO/EO/905

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication to Deposit Account No. 02-4377. A duplicate copy of this sheet is enclosed.

10/01/2001 SNAJARRO 00000038 09868797
01 FC:154 130.00 OP

Respectfully submitted,

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NY02:348218.1

A34394 PCT USA

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Matthias Weiss
Serial No.	:	To be Assigned
Filed	:	To be Assigned
For	:	DEVICE AND METHOD FOR GENERATING AND EXECUTING COMPRESSED PROGRAM OF A VERY LONG INSTRUCTION WORLD PROCESSOR

PRELIMINARY AMENDMENT

Assistant Commissioner of Patents

Washington, D.C. 20231

Sir:

Preliminary to the examination of the above-identified application, please make the following amendment to the claims:

In the Claims:

Cancel claims 1 to 10.

Add the following new claims 11 to 20.

11. A method for controlling functional units in a processor in a configuration, in which a sequence of primary instruction words consisting of multiple instruction word parts and originating from a translation of a program code is compressed and stored as a sequence of related program words, and according to which, in a subsequent execution phase, sequential secondary instruction words consisting of a plurality of instruction word parts and having the full instruction word width needed to control all functional units are generated from the sequence of program words, comprising:

as a result of the configuration, a program word has a first characteristic of a primary instruction word from a first group of preceding primary instruction words, which has the greatest similarity to the primary instruction word associated with the program word, and contains instruction word parts that differentiate the primary instruction word belonging to the program word from the primary instruction word belonging to the first characteristic;

in the execution phase, storing each instruction word in a second group of secondary instruction words corresponding in number to the first group is provided with a second characteristic;

in accordance with the first characteristic contained in the program word, ascertaining a secondary instruction word corresponding to the associated primary instruction word from the second group via the associated second characteristic; and

generating the secondary instruction word corresponding to the program word such that the instruction word parts contained in the program word are exchanged in the secondary instruction word from the second group.

12. The method in accordance with claim 11, wherein:

the first group consists of a first number of primary instruction words that directly precede the primary instruction word in question; and

the second group consists of a second number of secondary instruction words that is at least equal to the first number, where, prior to the generation of the next sequential secondary instruction word, each most recent secondary

instruction word is appended to the second group as the last word, and the first secondary instruction word to have been added and that is in excess of the second number is removed from the second group.

13. The method in accordance with claim 11, wherein the newly generated secondary instruction word is appended to the second group in that the former is stored in place of the secondary instruction word that was used for its generation.

14. The method in accordance with claim 11, wherein the newly generated secondary instruction word is not stored.

15. The method in accordance with 11, wherein the first characteristic is formed as a minimum code distance between the primary instruction word belonging to the program word in question and the primary instruction word with the greatest similarity.

16. The method in accordance with 11, wherein the second characteristic consists of an address corresponding to the first characteristic that is the address of a preceding secondary instruction word in a memory used for storage of the second group.

17. The method in accordance with claim 11, wherein the program word consists of a number of instruction word parts that corresponds to the number of instruction

word parts to be differentiated that occurs most frequently within the configuration, and in that a plurality of program words are used to assemble secondary instruction words that require more than the number of instruction words stored in one program word for the secondary instruction word used for generation.

18. The method in accordance with claim 11, wherein the instruction word parts are compressed in one program word by reducing the bit width to the extent that it is possible to represent the most frequently occurring instruction word parts; and in that multiple program words are used when instruction word parts occur that require a greater bit width in order to be represented.

19. The method in accordance with claim 18, wherein the width of the instruction word parts in the program word is halved, and one or two program words are provided for representation of the instruction word parts.

20. A processor arrangement for carrying out the method of claim 1, comprising:

a plurality of functional units;

an instruction word memory associated with the functional units; and

an instruction word buffer for storing instruction words that have already been generated and have a width that is at least the size of the bit width of the secondary instruction word; the instruction word buffer including a memory with selective line-by-line access.

REMARKS

This amendment eliminates multiple dependency in the claims and puts the claims in better U.S. format. No new matter is introduced by this amendment.

Respectfully submitted,

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[Translation from German]

WO 00/38049 PCT/DE99/04050

Device and Method for Generating and Executing Compressed Programs of a Very-Long-Instruction-Word Processor

Description

The invention relates to a method for controlling functional units in a processor, according to which, in a configuration, a sequence of primary instruction words consisting of multiple instruction word parts and originating from a translation of a program code is compressed and stored as a sequence of related program words. In a subsequent execution phase, sequential secondary instruction words consisting of a plurality of instruction word parts and having the full instruction word width needed to control all functional units are generated from the sequence of program words.

The invention also relates to a processor arrangement for carrying out the method having functional units, an instruction word memory associated with these functional units and an instruction word buffer for storing instruction words that have already been generated and have a width that is at least the size of the bit width of the secondary instruction word.

Processor arrangements of the aforementioned type contain functional units that operate in parallel to one another and that are controlled at every clock cycle by an instruction word. The particular instruction word is extracted from a program word that is taken from a program memory.

For their part, the instruction words consist of a plurality of instruction word parts, where each individual instruction word part serves to control one functional unit.

To improve the performance of processor arrangements, the goal is an increase in the processing width, which makes it necessary to increase the number of functional units. In general, this increases the bit width of the instruction words and thus also of the program words. The consequence of this is the provision of corresponding storage space in the program memory, which occupies the majority of the area on the semiconductor chip.

Since the size of the program words determines the size of the program memory, the goal is to reduce the size of the program words in order to reduce the need for memory space. A number of compression methods for this purpose are known. The most obvious method is described in the report by H. Weiss and G. Fettweis, [in English:] "Dynamic Codewidth Reduction for VLIW Instruction Set Architectures in Digital Signal Processors" (Proceedings of the 3rd International Workshop on Signal and Image Processing IWSIP '96, pages 517 to 520).
In this method, the program words are assembled from sequential primary instruction words in such a way that secondary instruction words can be subsequently reproduced therefrom in that a secondary instruction word (VLIW),

once it has been created, is written to an instruction word memory, and, in order to produce the next secondary instruction word, only those instruction word parts in the stored secondary instruction word are exchanged which differ between the stored secondary instruction word and the secondary instruction word to be generated. Consequently, the program word need only contain the information specifying which instruction word part differs and with what content it differs. It is thus possible to design the program words to be very narrow and thus save memory space.

However, when there are great differences between the stored secondary instruction word and the secondary instruction word to be created, the width of the program word must be increased if these relatively great differences occur frequently, which entails the disadvantage of a relatively large memory space, or else the differences must be distributed over multiple program words. Thus, the secondary instruction word must be created from multiple program words over multiple clock cycles. This results in the disadvantage that it requires a relatively long time.

Hence, the object of the invention is to increase operating speed in an application-specific manner while retaining a small program word width.

As regards the method, the object is attained in that, as the result of the configuration a program word contains a first characteristic of a primary instruction word from a first group of preceding primary instruction words which has the greatest degree of correspondence with the primary instruction word associated with the program word, and contains instruction word parts which

differentiate the primary instruction word belonging to the program word from the primary instruction word belonging to the characteristic. In the execution phase, a second group — corresponding in number to the first group — of secondary instruction words, each of which is equipped with a second characteristic, is stored. By means of the first characteristic contained in the program word, a secondary instruction word corresponding to the associated primary instruction word is ascertained from the second group via the associated second characteristic, and the secondary instruction word corresponding to the program word is generated in that the instruction word parts contained in the program word are exchanged in the secondary instruction word from the secondary group.

As early as the configuration phase, the program words can be constructed such that they contain only the minimum possible information for later generation of a secondary instruction word in the execution phase. This is achieved by referring back to the preceding primary instruction words that have the greatest correspondence with the primary instruction word to be configured. Since the secondary instruction words are to be generated during the execution phase with the same width and in the same sequence as the primary instruction words, the execution phase proceeds essentially in the reverse order to the configuration phase, and the already generated secondary instruction words corresponding to the primary instruction word most similar in the configuration phase to a current primary instruction word are used one at a time to generate a new secondary instruction word. Since the instruction word with the greatest similarity or the greatest correspondence is always referred back to, the amount

of information necessary to generate a new secondary instruction word can be kept as small as possible. In this way, it is possible to minimize the storage requirement of a program memory.

In one embodiment of the method, provision is made for the first group to consist of a first number of primary instruction words directly preceding the primary instruction word in question. The second group consists of a second number of secondary instruction words that is at least equal to the first number, where, prior to the generation of the next sequential secondary instruction word, the most recent secondary instruction word is appended to the group as the last word, and the first secondary instruction word to have been added that is in excess of the second number is removed from the second group. The group thus always consists of the immediately preceding instruction words, one of which has a greatest possible similarity when the instruction words within a group differ in content.

Another possible embodiment of the method is for the newly generated secondary instruction word to be appended to the second group in that this word is stored in place of the secondary instruction word that was used to generate it.

This variant of the process precludes the possibility of the group filling up with instruction words having the same content when the same function is passed through multiple times.

Another possibility is that the newly generated secondary instruction word is not stored. In this case, the same set of previously generated instruction words is always accessed each time a secondary instruction word is generated,

which is advantageous when these stored instruction words are suitable as pattern words for the generation of other secondary instruction words, with the result that storage processes can be avoided by this means.

In one embodiment of the method, provision is made for the first characteristic to be formed as a minimum code distance between the primary instruction word belonging to the program word in question and the primary instruction word with the greatest similarity.

Another embodiment of the method provides for the second characteristic to consist of an address corresponding to the first characteristic that is the address of a preceding secondary instruction word in a memory used for storage of the second group.

Both of these embodiments exhibit an especially simple generation of features.

A reduction in the program word width, and thus an associated reduction in the width of the program memory, can be achieved in that the program word consists of a number of instruction word parts that corresponds to the number of instruction word parts to be differentiated which occurs most frequently within the configuration, and in that a plurality of program words are used to assemble secondary instruction words that require more than the number of instruction words stored in one program word for the secondary instruction word used for generation. Consequently, the width of the program memory satisfies the most common application cases, and no delay arises in the generation of secondary instruction words. Only in the relatively few cases where the number of

instruction word parts to be changed exceeds the width of a program word are two or more program words required in two or more clock cycles to produce the secondary instruction word.

A further reduction in program word width can be achieved in that the instruction word parts are compressed in one program word. This is accomplished in that the bit width is reduced to the extent that it is possible to represent the most frequently occurring instruction word parts, and in that multiple program words are used when instruction word parts occur that require a greater bit width in order to be represented.

For this type of compression of the program word, it is especially useful for the width of the instruction word parts in the program word to be halved and for one or two program words to be provided for representation of the instruction word parts. For example, if the program word normally has a width of 8 bits, 256 combinations are available. However, a large number of these combinations is required only extremely rarely or not at all. Accordingly, the program word can be provided with a width of 4 bits, which is sufficient to represent the 16 most frequently occurring combinations. If a combination other than these should need to be represented, two or more program words are used for this purpose. However, since this occurs only very rarely, the savings in storage space for the program memory that is achieved is greater than the possible expenditure of time for generation of rare combinations.

The object is also achieved in accordance with the invention by a processor arrangement that is characterized in that the instruction word buffer

consists of a memory with selective line-by-line access. In contrast to the prior art shown, this affords the possibility of directly accessing various stored instruction words in order to produce a new secondary instruction word. Thus, it is not necessary to use just any stored instruction word for generating a new secondary instruction word, but rather the particular stored instruction word can be used that has the greatest similarity to the secondary instruction word to be generated. Hence, the resource requirements for changes are relatively small, requiring only a small bit width for the program word, and thus a small program memory.

The invention is described in detail below with reference to an example embodiment. The appertaining drawings show:

Fig. 1 a flowchart of the inventive method, and

Fig. 2 the principle of the inventive generation of the primary and secondary instruction words.

In the method represented in Fig. 1 for control of functional units 1 in a processor 2, a sequence of primary instruction words 5 is generated from a plurality of instruction word parts 6 from a program code 3 by means of a translation 4 in a configuration phase. This sequence of primary instruction words 5 is compressed and stored in a program memory 8 as a sequence of related program words 7.

The program words 7 consist of a number of instruction word parts 6 corresponding to the most frequently occurring number of instruction words 6 to

be differentiated within the configuration. In order to compose secondary instruction words 9, more than the number of instruction word parts 6 stored in one program word 7 may be needed. Then a plurality of program words 7 are used to do so.

In a subsequent execution phase, sequential secondary instruction words 9 consisting of a plurality of instruction word parts 6 and having the full instruction word width needed to control all functional units 1 are generated from the sequence of program words 7.

In the result of the configuration, a program word 7 has a first characteristic 10 of a primary instruction word 5 from a first group 11 of preceding primary instruction words 5, which has the greatest similarity to the primary instruction word 5 associated with the program word 7, and contains instruction word parts 6 that differentiate the primary instruction word 5 belonging to the program word 7 from the primary instruction word 5 belonging to the characteristic. The first characteristic 10 is formed as a minimum code distance between the primary instruction word 5 belonging to the relevant program word 7 and the primary instruction word 5 with the greatest similarity.

In the execution phase, a second group 12 of secondary instruction words 9 — corresponding in number to the first group 11 — each of which is provided with a second characteristic 13, is stored. The second characteristic 13 is formed from a line number of a memory 14 that serves to store the second group 12.

By means of the first characteristic 10 contained in the program word 7, a secondary instruction word 9 corresponding to the associated primary instruction word 5 is ascertained from the second group 12 via the associated second characteristic 13. The secondary instruction word 9 corresponding to the program word is generated in that the instruction word parts 6 contained in the program word 7 are exchanged in the secondary instruction word 9 from the second group 12.

The first group 11 consists of a first number of the primary instruction words 5 preceding the primary instruction word 5 in question. The second group 12 consists of a second number of secondary instruction words 9, which is at least equal to the first number, where, prior to the generation of the next sequential secondary instruction word 9, each most recent secondary instruction word 9 can be appended to the second group 12 as the last word. The first secondary instruction word 9 to have been added that is in excess of the second number is removed from the second group 12.

Method for controlling functional units in a processor and processor arrangement for carrying out the method

List of Symbols

1	functional unit
2	processor
3	program code
4	translation
5	primary instruction word
6	instruction word part
7	program word
8	program memory
9	secondary instruction word
10	first characteristic
11	first group
12	second group
13	second characteristic
14	memory

Claims

1. Method for controlling functional units in a processor, according to which, in a configuration, a sequence of primary instruction words consisting of multiple instruction word parts and originating from a translation of a program code is compressed and stored as a sequence of related program words, and according to which, in a subsequent execution phase, sequential secondary instruction words consisting of a plurality of instruction word parts and having the full instruction word width needed to control all functional units are generated from the sequence of program words **characterized in that**,

in the result of the configuration, a program word (7) has a first characteristic (10) of a primary instruction word (5) from a first group (11) of preceding primary instruction words (5), which has the greatest similarity to the primary instruction word (5) associated with the program word (7), and contains instruction word parts (6) that differentiate the primary instruction word (5) belonging to the program word (7) from the primary instruction word (5) belonging to the first characteristic (10)

and in that, in the execution phase, a second group (12) of secondary instruction words (9) — corresponding in number to the first group (11) — each of which is provided with a second characteristic (13), is stored, and

in that, by means of the first characteristic (10) contained in the program word (7), a secondary instruction word (9) corresponding to the associated primary instruction word (5) is ascertained from the second group (12) via the associated second characteristic (13), and the secondary instruction word (9) corresponding to the program word (7) is generated in that the instruction word parts (6) contained in the program word (7) are exchanged in the secondary instruction word (9) from the second group (12).

2. Method in accordance with claim 1, **characterized in that** the first group (11) consists of a first number of primary instruction words (5) that directly precede the primary instruction word (5) in question and

in that the second group (12) consists of a second number of secondary instruction words (9) that is at least equal to the first number, where, prior to the generation of the next sequential secondary instruction word (9), each most recent secondary instruction word (9) is appended to the second group (12) as the last word, and the first secondary instruction word (9) to have been added and that is in excess of the second number is removed from the second group (12).

3. Method in accordance with claim 1, **characterized in that** the newly generated secondary instruction word (9) is appended to the second

group (12) in that the former is stored in place of the secondary instruction word (9) that was used for its generation.

4. Method in accordance with claim 1, **characterized in that** the newly generated secondary instruction word (9) is not stored.

5. Method in accordance with one of claims 1 through 4, **characterized in that** the first characteristic (10) is formed as a minimum code distance between the primary instruction word belonging to the program word in question and the primary instruction word with the greatest similarity.

6. Method in accordance with one of claims 1 through 5, **characterized in that** the second characteristic (13) consists of an address corresponding to the first characteristic that is the address of a preceding secondary instruction word in a memory (14) used for storage of the second group (12).

7. Method in accordance with one of claims 1 through 6, **characterized in that** the program word (7) consists of a number of instruction word parts (6) that corresponds to the number of instruction word parts (6) to be differentiated that occurs most frequently within the configuration, and in that a plurality of program words (7) are used to assemble secondary instruction words (9) that require more than the number of instruction

words (9) stored in one program word (7) for the secondary instruction word (9) used for generation.

8. Method in accordance with one of claims 1 through 7, **characterized in that** the instruction word parts (6) are compressed in one program word (7) by reducing the bit width to the extent that it is possible to represent the most frequently occurring instruction word parts (6), and in that multiple program words (7) are used when instruction word parts (6) occur that require a greater bit width in order to be represented.

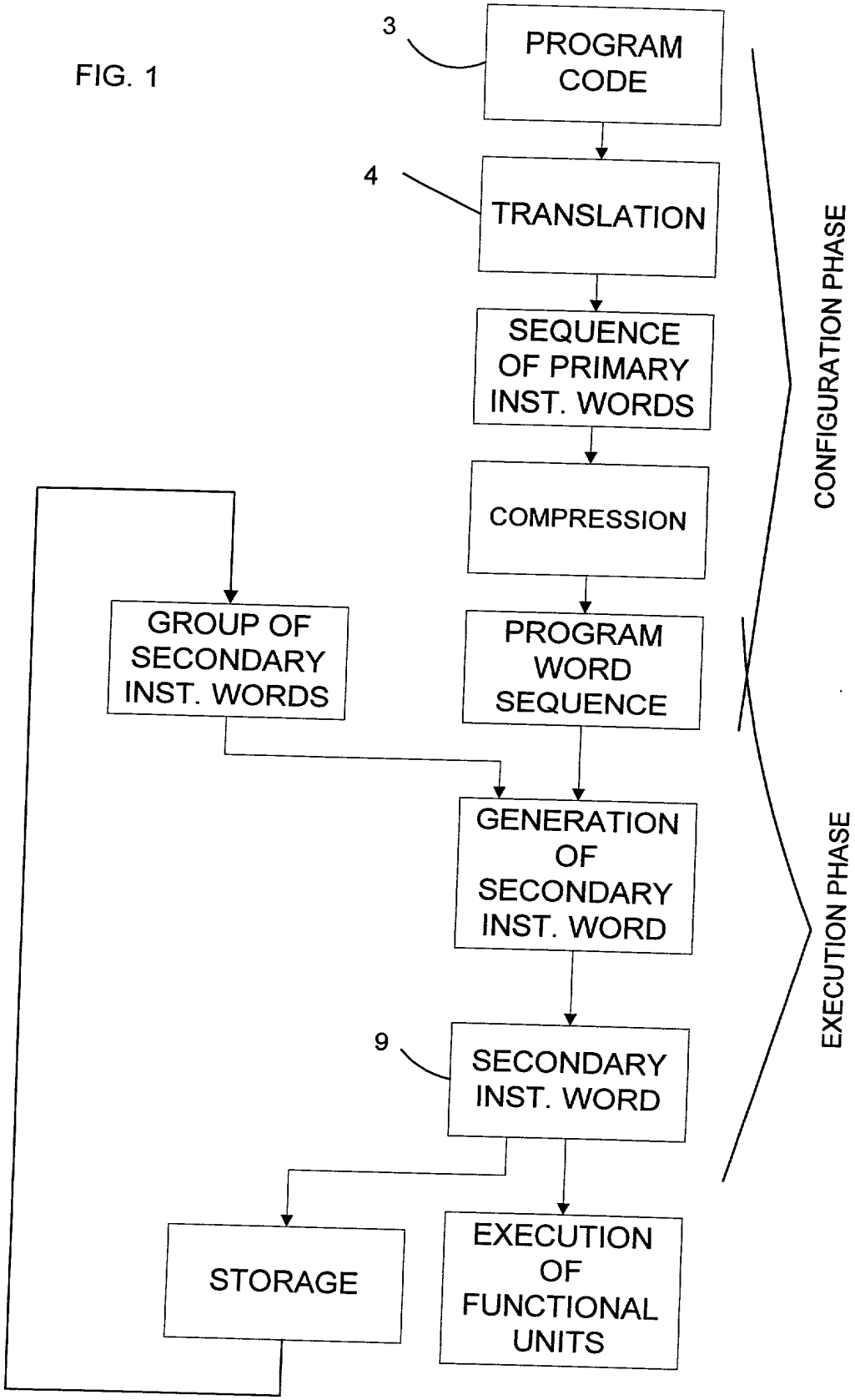
9. Method in accordance with claim 8, **characterized in that** the width of the instruction word parts (6) in the program word (7) is halved, and one or two program words (7) are provided for representation of the instruction word parts (6).

10. Processor arrangement for carrying out the method, having functional units, an instruction word memory associated with these functional units and an instruction word buffer for storing instruction words that have already been generated and have a width that is at least the size of the bit width of the secondary instruction word, **characterized in that** the instruction word buffer consists of a memory (14) with selective line-by-line access.

ABSTRACT OF THE DISCLOSURE

The invention relates to a method for controlling functional units in a processor, according to which in a configuration a sequence of primary instruction words which consists of several instruction word parts and originates from a translation of a program code is compressed and stored as a sequence of associated program words. The invention also relates to a processor system for carrying out this method. The aim of the invention is to increase operating speed in an application-specific manner while retaining a low program word width. To this end, as regards the method, a program word contains a first characteristic of a primary instruction word and instruction word parts which differentiate the primary instruction word belonging to the program word from the primary instruction word belonging to the characteristic. By means of the first characteristic contained in the program word a secondary instruction word is generated by exchanging the instruction word parts contained in the program word with those in a preceding secondary instruction word. On the system side the aim of the invention is solved by providing for the instruction word buffer to consists of a memory with optional line-by-line access.

FIG. 1



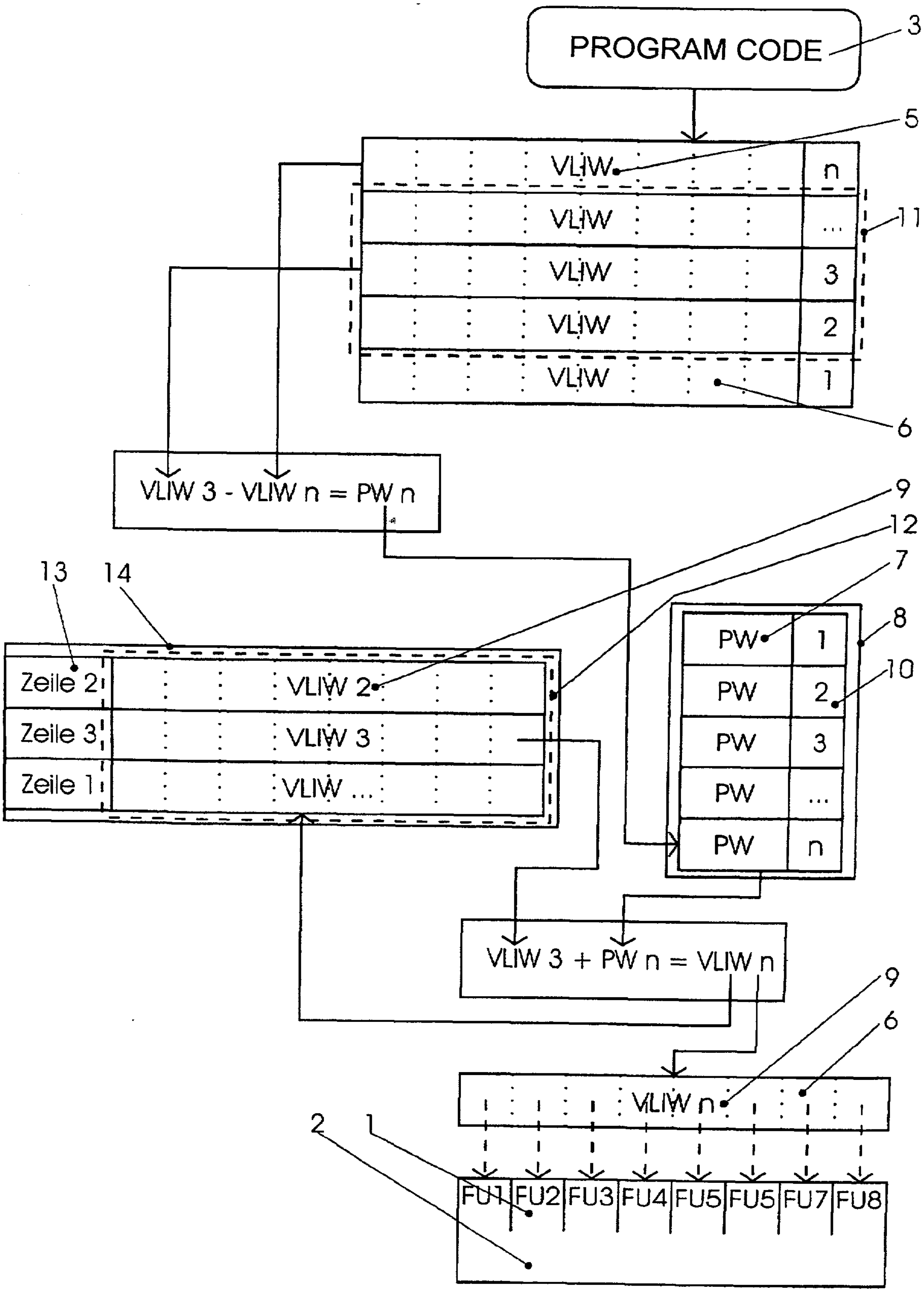


Fig. 2

COMBINED DECLARATION AND POWER OF ATTORNEY

(Original, Design, National Stage of PCT, Divisional, Continuation or C-I-P Application)

As a below named inventor, I hereby declare that: Matthias Weiss
My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

DEVICE AND METHOD FOR GENERATING AND EXECUTING COMPRESSED PROGRAMS OF A VERY LONG INSTRUCTION WORD PROCESSOR

This declaration is of the following type:

- [] Original
- [] Design
- [X] national stage of PCT.
- [] Divisional
- [] Continuation
- [] continuation-in-part (C-I-P)

the specification of which: (complete (a), (b), or (c))

(a) [] is attached hereto.
(b) [X] was filed on _Jun 21, 2001 as Application Serial No. _09/868,797 and was amended on (if applicable).
(c) [ ] was described and claimed in PCT International Application No. filed on and was amended on (if applicable).

Acknowledgement of Review of Papers and Duty of Candor

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of the subject matter claimed in this application in accordance with Title 37, Code of Federal Regulations § 1.56.

[] In compliance with this duty there is attached an information disclosure statement. 37 CFR 1.98.

Priority Claim

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or of any PCT International Application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT International Application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application on which priority is claimed

(complete (d) or (e)

(d) [] no such applications have been filed.
(e) [x] such applications have been filed as follows:

PRIOR FOREIGN/PCT APPLICATION(S) FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO SAID APPLICATION				
COUNTRY	APPLICATION NO.	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)	PRIORITY CLAIMED UNDER 35 USC 119
				[] YES NO []
				[] YES NO []
				[] YES NO []
ALL FOREIGN APPLICATION[S], IF ANY, FILED MORE THAN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO SAID APPLICATION				
Germany	198 59 389.9	22 December 1998		[x] YES NO []
International	PCT/DE99/04050	21 December 1999		[x] YES NO []
				[] YES NO []

Claim for Benefit of Prior U.S. Provisional Application(s)

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Provisional Application Number	Filing Date

Claim for Benefit of Earlier U.S./PCT Application(s) under 35 U.S.C. 120

(complete this part only if this is a divisional, continuation or C-I-P application)

(Application Serial No.)	(Filing Date)	Status (patented, pending, abandoned)

Power of Attorney

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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